

L Number	Hits	Search Text	DB	Time stamp
1	1384	phase near3 chang\$3 near3 device	USPAT;	2003/10/31 06:39
2	564	(phase near3 chang\$3 near3 device) and (gate electrode)	US-PGPUB	2003/10/31 06:39
3	174	((phase near3 chang\$3 near3 device) and (gate electrode)) and etch\$3	USPAT;	2003/10/31 06:24
4	732	phase near3 chang\$3 near3 device	US-PGPUB EPO; JPO; DERWENT; IBM_TDB	2003/10/31 06:39
5	53	(phase near3 chang\$3 near3 device) and (gate electrode)	EPO; JPO; DERWENT; IBM_TDB	2003/10/31 06:39
-	2202	tapered near5 electrode	USPAT;	2003/10/31 06:23
-	112	(tapered near5 electrode) and trench	US-PGPUB	2003/10/30 12:03
-	1182	tapered near5 electrode	USPAT;	2003/10/30 12:02
-	0	(tapered near5 electrode) and trench	US-PGPUB EPO; JPO; DERWENT; IBM_TDB	2003/10/30 12:02
-	0	(tapered near5 electrode) and (trench onen\$3 recess hole via contact)	USPAT;	2003/10/30 12:03
-	2000	(tapered near5 electrode) and (trench onen\$3 recess hole via contact)	US-PGPUB	2003/10/30 15:36
-	1645	tapered near5 electrode	USPAT;	2003/10/30 15:17
-	410	(tapered near5 electrode) and (trench onen\$3 recess hole via contact)	US-PGPUB EPO; JPO; DERWENT; IBM_TDB	2003/10/30 15:32
-	77	((tapered near5 electrode) and (trench onen\$3 recess hole via contact)) and (semiconductor wafer)	EPO; JPO; DERWENT; IBM_TDB	2003/10/30 15:32
-	2931	tapered near5 (electrode gate)	USPAT;	2003/10/30 15:36
-	2649	(tapered near5 (electrode gate)) and (trench onen\$3 recess hole via contact)	US-PGPUB	2003/10/30 15:36
-	1307	((tapered near5 (electrode gate)) and (trench onen\$3 recess hole via contact)) and (semiconductor wafer substrate)	USPAT;	2003/10/30 15:37
-	984	((tapered near5 (electrode gate)) and (trench onen\$3 recess hole via contact)) and (semiconductor wafer substrate) and etch\$3	USPAT;	2003/10/30 15:37
-	779	((tapered near5 (electrode gate)) and (trench onen\$3 recess hole via contact)) and (semiconductor wafer substrate) and etch\$3)	USPAT;	2003/10/30 15:45
-	4471	phase near10 change near10 (device memory)	US-PGPUB	2003/10/30 15:45
-	7	(phase near10 change near10 (device memory)) and (tapered near5 (electrode gate))	USPAT;	2003/10/30 15:46
-	4825	(gate electrode) near10 (etch\$3 pattern\$3) near100 mask near100 (trench hole open\$3 via contact recess groove)	US-PGPUB	2003/10/30 18:56
-	1481	((gate electrode) near10 (etch\$3 pattern\$3) near100 mask near100 (trench hole open\$3 via contact recess groove)) and charge	USPAT;	2003/10/30 18:56
-	1471	((gate electrode) near10 (etch\$3 pattern\$3) near100 mask near100 (trench hole open\$3 via contact recess groove)) and charge and (semiconductor wafer substrate)	USPAT;	2003/10/30 18:17
-	2095	(gate electrode) near10 (etch\$3 pattern\$3) near100 mask near100 (trench hole open\$3 via contact recess groove)	EPO; JPO; DERWENT; IBM_TDB	2003/10/30 18:56
-	45	((gate electrode) near10 (etch\$3 pattern\$3) near100 mask near100 (trench hole open\$3 via contact recess groove)) and charge	EPO; JPO; DERWENT; IBM_TDB	2003/10/30 18:57